REMARKS

I. Claim Rejection – 35 USC § 103

In a non-final Office Action, claims 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 were rejected under 35 USC § 103(a) as being unpatentable over Barkatullah in view of Neal. Applicants present the following arguments with respect to this rejection.

A. Amendment of Independent Claims

1. Upstream and downstream slave latches associated with master latch

Independent claims 1, 10, and 16 are amended above to incorporate parts of dependent claims 8, 14 and 21 and, so as to recite that the flip-flop includes a master latch and an upstream slave latch. Independent claim 28 already included these recited latches. This clarifies that the master latch is associated with not one, but two slave latches, with the two slave latches being coupled to opposed sides of the first level shifter. The triggering of the downstream slave latch is delayed relative to the triggering of the upstream slave latch by clock delays introduced by both (1) the second level shifter and (2) the delay element. The delay of the clock signal caused by second level shifter corrects in part for the delay of the level shifted data signal caused by the first level shifter; however, this clock delay of the second level shifter is insufficient by itself, due to a period of mismatch in the level shifted data signal. Consequently, the delay element introduces an additional clock delay to the delayed clock signal so as to trigger the downstream slave latch after the period of mismatch in the level shifted data signal caused by the first level shifter. The additional delay provided by the delay element is described in Paragraphs 0019 and 0020 of Applicants's specification as follows:

> "The added delay of the delay element 54 may be set to insure that the downstream slave latch 56 does not become transparent (open state) and pass the Level Shifted Data signal until after the period of mismatch shown in the Level Shifted Data signal. In other words, the downstream slave latch 56 remains non-transparent (close state) until after the rising and falling data edges

of the Level Shifted Data signal from the first level shifter 50 have arrived and been set up at the downstream slave latch 56 so that the period of mismatch has passed. Then, after the period of mismatch, a single clock edge of the Level Shifted Clock signal is used to trigger the downstream slave latch 56 to transition from its close state to its open state. ….Another way to characterize this delay is that the downstream slave latch 56 is waiting for the slowest of the rising and falling data edges to arrive before transitioning to its open or transparent state."

2. Using a single clock edge for downstream slave latch

Independent claims 1, 10, 16, and 28 have been amended by reciting that the clock signal has two clock edges, a "triggering clock edge" and a "non-triggering clock edge". As is inherent in clock signals (also recited in dependent claims), the clock signal has two clock edges, a rising clock signal edge and a falling clock signal edge. This amendment in turn helps to clarify that the the recited "downstream slave latch" is triggered by a single clock edge of the clock signal (the recited "triggering clock edge") and therefore is not triggered by the non-triggering clock signal. In contrast, a downstream flip-flop put in place of the recited downstream latch would use both clock edges, one to trigger the master latch of the flip-flop and the other to trigger the slave latch of the flip-flop. In doing so, the flip-flop performs a different function than the downstream latch, as will be described later.

As recited in the specification in Paragraphs 0017-0018, this use of the downstream latch, triggered by a single clock edge, has the following significance:

"The first level shifter 30 generates at its output a Level Shifted Data signal shown in FIG. 4. The rising and falling data edges of the data transitions of the Level Shifted Data signal are mismatched due to Tco skew caused by the first level shifter 34, as shown by cross hatching. The cross hatching shows where a plurality of rising and falling data edges occur over a plurality of clock cycles. More specifically, the delays in the rise and fall times of the data transitions differ, with either one possibly being longer relative to the other, depending upon

the particular level shifter and the particular values of the voltage supply settings. It should be noted that this period of mismatching is generated by both the falling and rising data edges and is not generated by just the falling data edges or just the rising data edges. The period of mismatch of all rising data edges or all falling data edges would likely be considerably shorter in duration. Consequently, the signal variation caused one clock edge of the delayed Clock signal going through the second level shifter 52 is smaller than the variation caused by both the rising and falling data edges of the Data2 signal going through the first level shifter 50 or the rising and falling clock edges of the delayed Clock signal going through the second level shifter 52."

"Only a single triggering clock edge of Level Shifted clock signal is used for clocking the downstream slave latch 56. Although this triggering clock edge may be either the rising clock edge or falling clock edge, in the illustrative example it is arbitrarily selected to be the falling clock edge of the Level Shifted Clock signal. Hence, there is less skewing (signal variation) of the Level Shifted Clock signal, utilizing only one clock edge, than the Level Shifted Data signal, having both rising and falling data edges. More specifically, the falling edges of the Level Shifted Data signal and the Level Shifted Clock signal substantially match except for variations caused by noise. The largest mismatch will be the falling clock edge of the Level Shifted Clock signal and the rising data edge of the Level Shifted Data signal."

A more detailed description of these features and their operation may be found in Paragraphs 0017-0021 of Applicants' specification. Neither Barkatullah in view of Neal, singly or in combination disclose the above described and claimed features. Additionally, independent claims 1 and 28 were amended to include the second level shifter of dependent claims 2 and 30; hence, all independent claims now recite the second level shifter.

B. Response to Examiner's section entitled "Response to Arguments"

In the section of Examiner's Office Action entitled "Response to Arguments", the Examiner made a number of counter arguments, which Applicants will repeat and then specifically address below:

Examiner: "Neal teaches a delay element (signal deskewer 150) that is coupled between a level shifter (101) and microprocessor (105). The level shifter in Neal is present to shift the voltage level of both data signals (40la, 402a, 403a) and clock signal (160). The deskewer (150) of Neal is present to add a delay (T -t) to compensate for delay *(t)* caused by the level shifter. Neal further teaches that this deskewing realigns falling and rising edges of the clock being delivered to the microprocessor (column 5, lines 16-58). Therefore, Barkatullah in combination with Neal does teach a delay element to avoid a period of signal mismatching such that the clock signal of Barkatullah that is delivered to the flip-flop is delayed by the delay element of Neal to realign falling and rising edges of the clock delivered to said flip-flop."

> **Applicants' response**: This is a correct interpretation of Neal by the Examiner. However, the signal deskewer 150 has no teachings relevant to Applicants' claimed invention, because Applicants' claimed invention is totally differerent in structure and function. As previously described in more detail below, Neal is directed toward clock synchronization of the clock signals on the either side of a level shifter 101 by eliminating (compensating for) the delay t caused by the level shifter so that the clock phases of the clock signal on either side of the level shifter start and stop at the same time. To the contrary, the delay of the "second level shifter" of Applicants' claimed invention is not eliminated, but it is retained to compensate in part for the delay of the "first level shifter". More importantly, Applicants' claimed "delay element" adds additional clock delay to the clock delay of the second level shifter so as to further delay triggering of the downstream slave latch "until after an arrival of the signal transitions at the downstream slave latch". Since there are no relevant teachings in Neal to Applicants' claimed

invention in the independent claims, its combination with Barkatullah adds nothing to the rejection.

Examiner: “The Applicant further argues that neither Barkatullah nor Neal comprises a downstream latch at the output of the of the level shifter operates with a clocking delay relative to the flip-flop at the input of the level shifter to block a period of mismatch in the level shifted data signal. Examiner asserts, as argued above, Barkatullah in combination with Neal does teach the downstream latch (DFF3 as presented in previous Office Action in Barkatullah) at the output of the level shifter of Neal and further operates to delay the clock mismatch of the clock signals. (column 5, lines 16-58).

Applicants’ response: A flip-flop downstream (at the output) of a voltage level shifter, triggered by both clock edges of a non-delayed signal that has been synchronized with a clock source on the upstream side (input side) of the voltage level shifter, is not structually or functionally the same as a downstream slave latch, triggerred by a single delayed clock edge (the recited “triggering clock edge”), with the clock delay provided by the delay element, when combined with the clock delay of the second level shifter, being sufficient to exclude a period of mismatched (described in the claims as the “arrival of the rising and falling edges of the data signal”).

In other words, the downstream flip-flop DFF3 combination presented by the Examiner provides a wholly different function of latching the received data signal for one clock cycle using two clock edges that have been syncrohnized with the upstream clock source. With this flip-flop DFF3 combination, the timing of the synchronized clock edges would trigger the DFF3 prior to the completion of the period of mismatched. To the contrary, the claimed downstream slave latch of Applicants’ invention mirrors the operation of the upstream slave latch, except with a clock delay (not synchronized with the upstream slave latch) that cuts out the period of mismatch. Expressed yet another way, if the “clock signal” and

"delayed clock signal" was synchronized with the deskewer circuit of Neal, Applicants invention would not work to avoid the period of mismatch.

Examiner: "Also, Applicant argues that the downstream latch of Barkatullah (DFF3 noted above) is not the same as the latches described within the text cited (paragraph 16) from the Specification. - However, the cited text in the Specification draws attention to a master-slave latch (42 comprising 44 and 46) that differs from downstream latch (56) that has a pair of inputs coupled to the first level shifter and the delay element. Barkatullah in combination with Neal does teach this limitation. Applicant further argues that a flip-flop is not a simple, single latch having an open and close state. However, the D flip-flops depicted in Barkatullah (column 9, line 9 thru column 10, line 13) are edge-triggered D flip-flops dependent on the clocks which inherently necessitates an open and close state (transparent and hold)."

Applicants' Response: Applicants repeat the above response. It is not only the difference in structure and timing between downstream slave latch and a downstream flip-flop, but the function involved and the results obtained are wholly different, as described above. The Examiner has totally failed to show any structure or function relevant to an upstream slave latch and a downstream slave latch which are associated with a given master latch, but are on opposed sides of a data level shifter and are triggered at at different times so as to cut out a period of mismatch from the data level shifter.

Moreover, the Examiner is breaking up a physically component, a flip-flop (DFF3), and ignoring the fact that there is a master latch of the DFF3 flip-flop imposed between two slave latches in the Examiners' combination.

Examiner: "Furthermore, Applicant argues that the second level shifter is not present to generate a level shifted clock signal. Examiner asserts that the level shifter (101) of Neal accommodates for all signals (401,402 and 403) in addition to clock signal (160,

170) which internally necessitates a second level shifter to accommodate the entire level shifter circuit (101) (column 5, line 40 thru column 6, line 3)."

> **Applicants' Response**: This is an incorrect statement of Applicants' position as repeated below in Section II of this response, where Applicant stated that "Neal does teach using a level shifter for the clock signal, <u>as well as using a level shifter for the data signal</u>."

Examiner: "In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., different clock frequencies in the domains) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner would like to point out that Neal however, does not depict a clock generator that delivers different clock frequencies for the domains. Therefore, Barkatullah in combination with Neal does teach this limitation though it is not claimed. Lastly, Barkatullah in combination with Neal also teaches that the domains do have different voltage levels and voltage level shifters in the Applicants' invention such that the level shifter of Neal provides this detail to the clock signal and data signals (as depicted in above arguments).

> **Applicants' Response**: This is an incorrect statement of Applicants's position as repeated below in Section II of this Response, in that Applicants are in no way relying on claim recitations directed toward different clock frequencies in the two domains, nor is this distinction in anyway found in any of the dependent claims. To the contrary, Applicants independent claims merely recite different supply voltage sources, not sources having voltages with different frequencies – the frequencies of the two domains can be the same or different in Applicants' claimed invention. The point Applicants were making in the prior response was that Barkatullah (not Applicants' invention) merely teaches two clock signals with different frequencies in different domains; hence, it follows that there are no

teaching of two domains with different supply voltages in Barkatullah that would require voltage level shifters. In summary, this was a comment about the prior art, not the Applicants' invention – no different voltages, therefore no voltage level shifters.

II. Claim Rejection – 35 USC § 103

In this non-final Office Action, claims 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 were rejected under 35 USC § 103(a) as being unpatentable over Barkatullah in view of Neal, with the Examiner repeating his original positions from October 25, 2006 Office Action. In response to this, Applicants, to preserve Applicants' arguments for appeal and to be fully responsive to the Examiners' office action, repeat Applicants' responses provided in Applicants' November 24, 2006 response below:

A. No delay to avoid a period of data signal mismatch caused by a level shifter is disclosed or suggested in Barkatullah or Neal. Applicants' invention as claimed in the independent claims does not involve clock synchronization as undertaken in Barkatullah and Neal.

With respect to Barkatullah, the Examiner states that:

> "….a clock production circuit (Fig. 7) coupled to the clock source (102) and responsive to the clock signal (core clock) to generate a synchronized clock signal (bus clock) having a triggering edge….the clock production circuit (Fig. 7) is operable to synchronize an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch…"

With respect to Neal, the Examiner states that:

> "….a clock delaying mechanism (150) to synchronize clock triggering…. a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further delayed via delay element (150) … level shift both data and clock signal as well as delay the clock signal between domains for synchronization…."

Clock syncrhonization is commonly used in integrated circuits, but is not relevant to Applicants' invention as claimed in the independent claims 1, 10, 16, and 28. More specifically, the claimed "delayed clock signal" is not synchronized with the claimed "clock signal". To the contrary, Applicants' invention, as claimed in the independent claims, includes a delay sufficient to avoid the period of mismatch in the level shifted data signal, with that period of mismatch in the level shifted data signal being caused by the first level shifter. The period of mismatch is described in the independent claims by the claim language of "level shifted data signal has a plurality of rising and falling data edges".

Clock syncrhonization involves syncrhronization of a given clock signal with a reference clock signal. A simple example of this is illustrated in FIG. 4 of Neal and discussed in column 5, lines 16-39. There is shown a reference clock signal 300 (original clock that is an input to the voltage level shifter) and the delayed clock signal 302 (delay introduce by the voltage level shifter). By using a "signal deskewer", such as the signal deskewer 150 of FIG. 5, the delayed clock signal 302 is moved forward or backward to be concident with the original signal 300. This moved and synchronized clock signal is shown as signal 304 in FIG. 4.

In independent claims 10 and 16 and dependent claims 2 and 30, Applicants' recite the use of a second level shifter to generate a level shifted clock signal. Neal does teach

using a level shifter for the clock signal, as well as using a level shifter for the data signal. In the synchronization with the original clock signal 300, Neal teaches that the clock delay introduced by the voltage lever shifter for the clock signal is to be eliminated through clock synchronization. This leads to two distinctions:

(1) With respect to independent claims 1, 10, 16 and 28, in Neal the delay introduced by the clock level shifter at most would compensate for the delay introduced by the level shifter for the data signal (if the delay was not eliminated in Neal); however, that delay is insufficient by itself to block the period of signal mismatch caused by the level shifter for the data signal. Applicant's invention, as claimed in the independent claims, recites the delay element which adds sufficient delay to allow the downstream latch to block a period of mismatch in the data signal.

(2) With respect to independent claims 10 and 16 and dependent claims 2 and 30 reciting the second level shifter, the introduced clock delay of Applicants' invention not only includes the clock delay of the delay element, but also includes the clock delay of the second level shifter. Hence, the clock delay of the second level shifter is kept and used in Applicants's claimed invention, not eliminated by clock synchronization as taught by Neal.

In summary, the delay element of Applicants' invention introduces intended delay which is sufficient to eliminate the period of data signal mismatch. No such teaching is found in Neal.

In Barkatullah, clock synchronization becomes more involved, because of frequency translation in which there is a 2/N ratio of the bus clock signal to the core clock signal created by selecting every N/2 cycles of the core clock signal - there is some unrelated discussion as to which phase of the clock signals to use (e.g., see clock waveforms 201 and 202 in FIG. 6A). The Examiner recognizes that there is no delay element in

Barkatullah. Since there is no mismatch in a data signal from a level shifter in Barkatullah, then there is no need for the delay element to generate the delayed clock signal. Instead, the Examiner cites Neal for the delay element, which is not related to Applicants' delay element as described above.

In summary, neither Barkatullah and Neal, singly or in combination, disclose a delay element that delays a clock signal, which is used by a flip-flop at the input of a level shifter, to create a delayed clock signal, so as to block a period of signal mismatch caused by the level shifter by having a downsteam latch in a close state when receiving the period of signal mismatch and then triggering an open (transparent) state of the downstream latch with a triggering clock edge of the delayed clock signal after the arrival of signal mismatch. Neither Barkatullah and Neal, singly or in combination, disclose a delay element to delay a clock signal, with or without the delay of the second level shifter, to a sufficient degree to avoid the period of signal mismatch caused by a level shifter.

B. No downstream latch with open and close state in Barkatullah or Neal.

With respect to FIG. 8C of Barkatullah, the Examiner refers to the three series D flip-flops as DFF1, DFF2, and DFF3. Applicants will adopt the Examiner's characterization of these components in the discussion below. First, the Examiner takes two D flip-flops (DFF1 and DFF2) and states that this is Applicants' single claimed flip-flop. Second, the Examiner equates a third D Flip-flop (DFF3) to Applicants' "downstream latch having an open state and a close state". In doing so, the Examiner claims that the D flip-flop (DFF3), like Applicants' downstream latch, has an open state and a close state. This is a technically incorrect characterization of a flip-flop, with the proper description of a flip-flop being provided in paragraph 0016 of Applicants' specification, which will be repeated here:

"With respect to the master-slave flip-flop 42, the master and slave latches 44 and 46 each have an open and a close state. The latches 44 and 46 pass through the data when in the open (transparent) state and hold (latch) the data when in the close state. When the master latch 42 is in its close state, it is holding the Data1 signal acquired from the previous clock phase. At the same time, the slave latch 46 is in the open state and is passing the Data1 signal held by the master latch 42 through to the flip-flop's output as the Data2 signal. When the clock phase is reversed, the master latch 44 switches to its open state to acquire new Data1 signal and at the same time the slave latch 46 switches to its close state of holding the previous-provided Data1 signal and continuing to provide it at the output of the flip-flop 42 as the Data2 signal. Hence, the master and slave latches operate "out-of-phase". The rising clock edge of the clock signal shown in FIG. 4 may be used to reset the master latch 44 to its open state and the falling clock edge of the clock signal may be used to reset the slave latch 46 to its open state. Generally, the flip-flop 42 may introduce a one clock cycle delay in the Data1 signal to generate the Data2 signal."

Although each latch (master or slave) of the flip-flop (including a D flip-flop), has an open state, when the operation of the flip-flop is taken as a whole, a flip-flop does not have an open state, as made clear by the above-described "one clock cycle delay" of the flip-flop. This one clock cycle delay does not occur with the downstream latch, because during an open state of the dowstream latch the signal passes without delay and during the close state, the signal (including the period of signal mismatch) does not pass.

In summary, a flip-flop, including a D flip-flop, is not a simple, single latch having an open (transparent) state and close (hold or latch) state, but is a component that functions in a much different way, as described above. The downstream latch of Applicants' invention at the output of the level shifter operates with a clocking delay

relative to the flip-flop at the input of the level shifter to block a period of mismatch in the level shifted data signal.

No downstream latch is disclosed in Neal; hence, neither Barkatullah or Neal, singly or in combination discloses a downstream latch at the output of a level shifter.

C. Domains with different clock frequencies in Barkatullah versus domains with different voltage levels and voltage level shifters in Applicants' invention

FIG. 7 of Barkatullah shows a circuit for generating a bus clock signal, with one of the inputs being a core clock signal with a 2/N ratio between the bus clock signal to the core clock signal (column 2, lines 65-67, also FIG. 6A). DFF1 and DFF2 are provided a clock signal with one frequency (core clock) and DFF3 with another frequency (bus clock). Hence, Barkatullah is concerned with providing two clock signals of different frequencies to different domains, the bus clock domain and the core clock domain, as shown in FIG. 1. There are not two domains supplied with different supply voltages in Barkatullah; hence, there are no voltage level shifters, as the Examiner noted. To the contrary, Applicants' independent claims 1, 10, 16, 28 a "first supply voltage source" and a "second supply voltage source" and "a first level shifter".

Moreover, Applicants "clock signal" provided to the flip-flop has the same frequency as the "delayed clock signal" provided to the downstream latch, because they are the same signal but the delay introduced by the "delay element". In other words, the delay element does not change frequency, nor would Applicants' conveter circuit work if the frequency was changed. Hence, Barkatullah, with the exception of the clock source, does not teach any of the recited elements of Applicants' independent claims 1, 10, 16, 28.

D. Summary

Neither Barkatullah and Neal, singly or in combination, dislcose:

(1) a downstream slave latch at an output of a first level shifter, with the level shifter being interposed between an upstream slave latch of the flip-flop and the downstream slave latch; or

(2) a delay element, in combination with a second level shifter, to delay a clock signal used by the flip-flop, with the downstream latch using a single triggering clock edge of the delayed clock signal to switch the downstream latch from a close state to an open state after an arrival of the rising and falling data edges at the downstream latch.

III. Conclusion

Claims 1, 3-4, 7-11, 14-18, 21, 22, 28 and 31-32 are pending. Claims 2 and 30 were canceled in this office action response. Claims 5-6, 12-13,19-20, 23-27, and 29 were canceled in prior office action responses. In view of the foregoing amendments and arguments, Applicant submits that the pending claims are in condition of allowance. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 02/14/2007

/Aloysius T.C. AuYeung/
Aloysius T.C. AuYeung
Reg. No. 35,432

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981